Automatized Connection of the Layers of Planar Transformers with Parallel Windings to Improve the Component Behavior

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Abstract—**Transformers with parallel windings are commonly used to reduce the losses in the windings. Windings losses depend on the winding positioning and the frequency effects because each winding affects the current sharing of itself and the neighboring windings.**

In this paper a methodology for determining the connections of the parallel windings that reduces the power losses (and temperature) in the windings of multi-winding transformers is presented. Other applications of the method, such as balanced current sharing and voltage drop reduction are also explored.

I. Introduction

SMPS designers use planar components to reduce the parasitic elements of the magnetic components. Many planar transformers are designed and manufactured using parallel turns to reduce the resistance of the windings even more. The high frequency behavior of the magnetic component depends on many effects that must be evaluated to get an appropriate design: the working frequency, the geometry of the windings, their connections, and their loads.

This problem has been studied before [1-5]. In [1] a gapped transformer for a LLC resonant converter is designed, but this work lacks of a systematic search of windings connections. The advantages of using a solid turn or several turns in parallel area studied in [2] but using PCB layers several windings in parallel must be used to increase conductors sections. Analytical expressions for leakage inductance are presented in [3]. These expressions getting fast results, but an optimization procedure to get the best configuration is not used.

These limitations are avoided in the methodology developed in the present paper; the formulation of [6] to design gapped inductors with parallel windings has been modified for transformers with parallel windings in primary and secondary and a passive load in the secondary winding.

Section II presents the methodology to minimize the windings losses, in our opinion, the most useful application for the proposed methodology, but other applications of the method are presented in Section III. A transformer for a dc/dc converter was designed and built, and the design process and results are commented in Section IV.

II. Methodology to Obtain the Minimum Losses Windings Layout

The steps that should be followed to apply the proposed method are as follows:

Step 1: Design the magnetic component.

It is necessary to design the planar transformer in terms of selection of the core size and material, the number of turns and number of parallel layers of the winding. The windings will be contained in a multilayer PCB that should fill a large part of the core window in order to have enough space for the parallel windings and a large enough conductor section to reduce the windings resistance.

As an example, a two winding planar transformer is considered. The section of the windings and a schematic representation of the layer connections are represented in Figure 1.

The component that is represented is a N_1:N_2 = 3:1 transformer where each layer contains a turn. Primary is made of one winding (A) with three layers in series (3 turns) and secondary of three parallel windings (B, C, and D) of one layer each (1 turn).

The total number of layers in the PCB is six, three for the primary and three for the secondary. The proposed

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methodology allows sorting them to obtain the benefits indicated in the abstract.

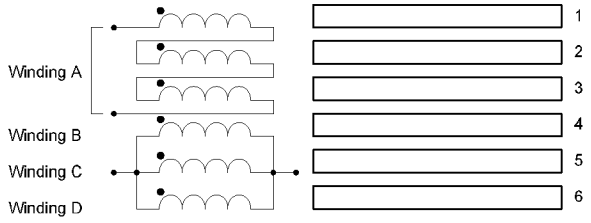

Figure 1. Connected layers of the design example.

Step 2: Obtain the complex impedances of the layers.

The self and mutual complex impedances of the individual layers of the transformer are calculated assuming that all the layers are disconnected. Figure 2 shows the example transformer with its windings disconnected. Now a six winding transformer with a turn in each winding is considered (N_1:N_2:N_3:N_4:N_5:N_6 = 1:1:1:1:1:1).

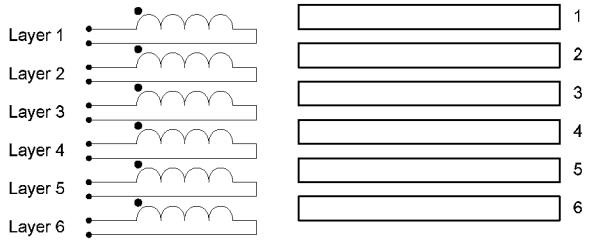

Figure 2. Unconnected layers of the design example.

As the current carried by a layer is affected by its location in the PCB, a layer close to the surface of the PCB behaves differently than a layer inside the PCB. Also, a high working frequency increases this effect. Finite Element Analysis (FEA) is used in this work to evaluate these effects [7], but analytical models [3] can be used to calculate these impedances.

It must be remarked, and it is a key aspect of the proposed methodology, that FEA (or any other selected method to calculate the impedance value) is used only one time for the calculation of these self and mutual layer impedances. Once these impedances are known, FEA is not necessary again, because the same layers in the same positions (and therefore, the same self and mutual impedances) are used during the whole optimization process to get a good connection of the layers. (The optimization methodology consists on changing the connections of layers that occupy the same positions always.) Therefore, the optimization procedure is very fast: a great number of layers connections can be evaluated in very short time to obtain the optimal solution.

Step 3: Evaluate layer connections to find the best one.

Once the self and mutual impedances of the individual layers are known, the self and mutual impedances of the windings can be calculated.

One possible winding layout is that of Figure 1, but more configurations with a primary with three series turns and a secondary with three parallel windings of one turn each are possible. This paper does not propose a method to select the layer configurations. For a low number of layers, all connections can be evaluated and for a high number of layers, designers should choose a rule to reduce the number of possibilities. For the configuration depicted in Figure 1, the layers of the windings are indicated in Table I.

TABLE I. LAYERS FOR THE PARALLEL WINDINGS OF FIGURE 1.

Winding	Layers
A	1-2-3
B	4
C	5
D	6

As an example, the self and mutual impedances for windings A and B are calculated using the expressions in (1). Is should be taken into account that the windings are coupled impedances, despite Figure 2 represents them as inductors or windings:

$$\underline{Z}_{AA} = \underline{Z}_1 + \underline{Z}_2 + \underline{Z}_3 + 2\,\underline{Z}_{12} + 2\,\underline{Z}_{13} + 2\,\underline{Z}_{23}$$

$$\underline{Z}_{BB} = \underline{Z}_4 \qquad (1)$$

$$\underline{Z}_{AB} = \underline{Z}_{14} + \underline{Z}_{24} + \underline{Z}_{34}.$$

Similar expressions can be derived for the remaining self and mutual impedances: $\underline{Z}_{AC}$, $\underline{Z}_{AD}$, $\underline{Z}_{BC}$, $\underline{Z}_{BD}$, $\underline{Z}_{CC}$, $\underline{Z}_{CD}$, and $\underline{Z}_{DD}$.

Once the model of the individual windings has been obtained, currents for this particular configuration are obtained analyzing the circuit in Figure 3. Once voltages and currents are known, the windings power losses can be obtained. Windings, represented as inductors in the figure, are a set of coupled impedances that are calculated using equations like those in (1).

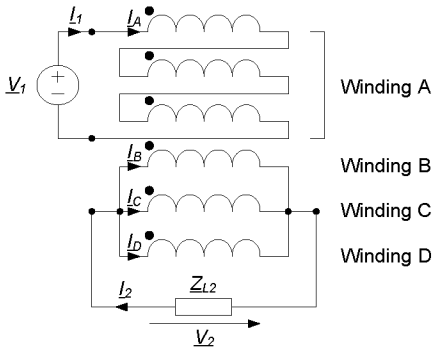

Figure 3. Currents calculation in the design example.

The system of equations (2) represents the couplings among all the parallel windings: A, B, C, and D. These

equations allow calculating the currents of windings A, B, C, and D if the winding voltages $\underline{V}_1$ and $\underline{V}_2$ are known.

$$\begin{pmatrix} \underline{V}_A \\ \underline{V}_B \\ \underline{V}_C \\ \underline{V}_D \end{pmatrix} = \begin{pmatrix} \underline{V}_1 \\ \underline{V}_2 \\ \underline{V}_2 \\ \underline{V}_2 \end{pmatrix} = \begin{pmatrix} \underline{Z}_{AA} & \underline{Z}_{AB} & \underline{Z}_{AC} & \underline{Z}_{AD} \\ \underline{Z}_{BA} & \underline{Z}_{BB} & \underline{Z}_{BC} & \underline{Z}_{BD} \\ \underline{Z}_{CA} & \underline{Z}_{CB} & \underline{Z}_{CC} & \underline{Z}_{CD} \\ \underline{Z}_{DA} & \underline{Z}_{DB} & \underline{Z}_{DC} & \underline{Z}_{DD} \end{pmatrix} \begin{pmatrix} \underline{I}_A \\ \underline{I}_B \\ \underline{I}_C \\ \underline{I}_D \end{pmatrix} \quad (2)$$

All currents enter the dotted terminals in this formulation. The current of winding 1 (primary) is $\underline{I}_1 = \underline{I}_A$ and the current of winding 2 (secondary) is $\underline{I}_2 = \underline{I}_B + \underline{I}_C + \underline{I}_D$, as Figure 3 illustrates. Note that all secondary windings B, C, and D have the same voltage, $\underline{V}_2$ because they are in parallel.

The voltage of winding 1 $\underline{V}_1$ is known and $\underline{V}_2$, the voltage of winding 2, can be calculated using the load impedance $\underline{Z}_{L2}$ and its current $\underline{I}_2$:

$$\underline{V}_2 = -\underline{Z}_{L2}\,\underline{I}_2 = -\underline{Z}_{L2}\,(\underline{I}_B + \underline{I}_C + \underline{I}_D) \quad (3)$$

Replacing (3) in (2), currents $\underline{I}_A$, $\underline{I}_B$, $\underline{I}_C$, and $\underline{I}_D$ can be obtained solving a linear system of equations, and power losses can be calculated using the following equation:

$$P_1 = \underline{V}_1\,\underline{I}_1 + \underline{V}_2\,\underline{I}_2 \quad (4)$$

As mentioned above, $\underline{I}_1 = \underline{I}_A$, $\underline{I}_2 = \underline{I}_B + \underline{I}_C + \underline{I}_D$, $\underline{V}_1$ is known, and $\underline{V}_2$ is calculated using (3).

The final step of the optimization process consists in selecting different layers connections, and obtaining the power losses using (4). The layer connection which produces the lowest power losses is the optimal solution. In some designs the optimal solutions could be inadequate, as connections could made very difficult the transformer manufacturing. In these cases, the proposed methodology gives the designer a set of winding connections with low losses and different interleaving levels. The designer can chose among them one that can be manufactured with low trouble.

Finally, note that the FEA process is run only one time for the layer impedances calculation in Step 2; the calculations in Step 3 are based on analytical expressions.

This methodology was implemented in a Matlab program. The program analyzes a very high number of configurations, presenting the best results to the user. As a usage example, a 1:12 transformer for a bridge converter was optimized using this program. The windings are in a 20 layer PCB with a thickness of 105 µm each. Primary has 4 parallel windings (A, B, C, and D) and secondary has 3 (E, F, and G). Table II shows the layers that connected in series make each parallel winding and the corresponding winding losses for the base design and the optimized one. A 7.6% loss reduction was obtained using this method.

TABLE II. BASE AND OPTIMIZED LAYER CONNECTIONS FOR LOSSES REDUCTION IN THE DESIGN EXAMPLE OF SECTION III.

Design	Primary layers	Secondary layers	Power losses (W)
Base	A: 5-6 B: 7-8 C: 13-14 D: 15-16	E: 1-2-3-4 F: 9-10-11-12 G: 17-18-19-20	1.3
Optimized	A: 7-8 B: 15-16 C: 6-13 D: 5-14	E: 4-11-18-20 F: 2-12-17-19 G: 1-3-9-10	1.2

III. OTHER APPLICATIONS OF THE METHODOLOGY

The methodology was used in the previous section to reduce power losses, but it is adequate to optimize using different criteria. Here, current sharing balancing and voltage drop reduction are commented.

A. Balancing the Current Sharing among Parallel Windings

The currents $\underline{I}_B$, $\underline{I}_C$, and $\underline{I}_D$ obtained solving (2) in Step 3 of the optimization procedure can be used to balance the current sharing among the parallel windings if solutions with similar currents in the parallel windings are selected during the optimization process explained in Section II.

As an example, the 1:12 transformer of the previous example was optimized using this new strategy. Table III indicates the layers of the parallel windings in primary and secondary. The optimized designs of tables II and III are not the same in order to accomplish the different objectives. In any case, the parallel windings are much interleaved.

TABLE III. BASE AND OPTIMIZED LAYER CONNECTIONS FOR BALANCED CURRENT SHARING IN THE DESIGN EXAMPLE OF SECTION III.

Design	Primary layers	Secondary layers
Base	A: 5-6 B: 7-8 C: 13-14 D: 15-16	E: 1-2-3-4 F: 9-10-11-12 G: 17-18-19-20
Optimized	A: 6-8 B: 5-7 C: 13-15 D: 14-16	E: 3-4-12-19 F: 2-9-17-18 G: 1-10-11-20

Primary has 4 parallel windings (A, B, C, and D) and secondary has 3 (E, F, and G). The windings are in a 20 layer PCB with a thickness of 105 µm each.

Table IV shows the currents in the windings for the base design. Note that current in parallel winding A and D exceed in a 14% the currents of parallel windings B and C, and the current of parallel winding F exceeds in a 122% the current of parallel windings E and G.

The optimized design presents a very balanced current sharing, as Table V shows. Two parallel windings of the primary exceed in a 7% the current of the other two parallel windings, but the currents of the parallel windings in the secondary are very similar.

TABLE IV. LAYERS AND CURRENTS FOR THE BASE DESIGN EXAMPLE IN SECTION III.

Winding	Layers	Current (A)
A	5-6	6.617511
B	7-8	5.830528
C	13-14	5.830384
D	15-16	6.617603
E	1-2-3-4	0.493826
F	9-10-11-12	1.088227
G	17-18-19-20	0.493865

TABLE V. LAYERS AND CURRENTS FOR THE OPTIMIZED DESIGN EXAMPLE IN SECTION III.

Winding	Layers	Current (A)
A	6-8	6.484022
B	5-7	6.052420
C	13-15	6.052439
D	14-16	6.483398
E	3-4-12-19	0.692985
F	2-9-17-18	0.693031
G	1-10-11-20	0.683156

B. *Reducing the Transformer Voltage Drop*

Voltage drop is calculated using (5), where $r_t = N_1/N_2$ and V_1 and V_2 are the rms voltages of windings 1 and 2.

$$\varepsilon = \frac{V_1 - r_t V_2}{V_1} \tag{5}$$

Voltage drop is an indicative of the value of the short-circuit impedance: transformers with high short-circuit impedances have high voltage drops.

This parameter can be diminished if designs that reduce (5) are selected during the optimization procedure.

IV. DESIGN AND CONSTRUCTION OF A TRANSFORMER PROTOTYPE USING THE PROPOSED METHODOLOGY

A transformer for a full bridge transformer was designed and built using the methodology proposed in this paper. A software tool, PExprt from Ansys [8], was used to make the preliminary design (Step 1 of the procedure). A sinusoidal primary voltage of 80 kHz, 18 V (rms) and a load resistance of 104 Ω were used to design this component. Summarized: these are the constructive characteristics of this design:

- Primary winding has three parallel windings (A, B, and C) made of two layers of 1 turn each connected in series (Its number of turns is $N_1 = 1 + 1 = 2$).
- Secondary winding has 4 parallel windings (D, E, F, and G) of two layers of 12 turns each connected in series (Its number of turns is $N_2 = 12 + 12 = 24$).
- A low profile planar Ferroxcube 3C90 EI core (32/6/20) was chosen.
- The 105 µm technology of the previous examples was used again, but this time, windings are placed in a 14-layer PCB to fit in the low profile EI core.

The current sharing balancing method explained in Section III is used to optimize the component design.

Some default interleaving is assigned before optimization to improve the coupling among windings: primary layers occupy positions 3, 4, 7, 8, 11, and 12, and secondary layers are 1, 2, 5, 6, 9, 10, 13, and 14.

The input and output electrical parameters used in the preliminary design: a sinusoidal primary voltage of 80 kHz, 18 V (rms) and a load resistance of 104 Ω were used for the optimization process.

Table VI shows the layers that compose primary and secondary windings of the base and optimized designs. Note the interleaving in the optimized design that permits improving the current sharing of the parallel windings of primary and secondary.

TABLE VI. BASE AND OPTIMIZED CONNECTIONS FOR CURRENT BALANCING.

Design	Primary layers	Secondary layers
Base	A: 3-4 B: 7-8 C: 11-12	D: 1-2 E: 5-6 F: 9-10 G: 13-14
Optimized	A: 3-7 B: 4-11 C: 8-12	D: 1-6 E: 2-10 F: 5-13 G: 9-14

Table VII shows that current is not shared equally among the parallel windings in the base design: note that the current of parallel winding B is an 18% lower than the current of parallel windings A or C and the current of windings D or G is a 40% lower than the current of parallel windings E or F.

TABLE VII. BASE DESIGN CURRENTS.

Winding	Layers	Current (A)
A	3-4	8.795694
B	7-8	7.210595
C	11-12	8.795186
D	1-2	0.393686
E	5-6	0.646761
F	9-10	0.646777
G	13-14	0.393602

The optimized design presents an almost equal current sharing among parallel windings as Table VIII indicates. Primary windings currents are almost equal and so do secondary winding currents.

TABLE VIII. OPTIMIZED DESIGN CURRENTS.

Winding	Layers	Current (A)
A	3-7	8.229651
B	4-11	8.342383
C	8-12	8.229433
D	1-6	0.506719
E	2-10	0.527306
F	5-13	0.527337
G	9-14	0.506782

Figure 4 shows the measured short-circuit resistance and inductance of the component. Resistance and inductance from the secondary winding at 80 kHz are 863.75 mΩ and 2.92 µH respectively. These parasitic effects are adequate for the designed power converter.

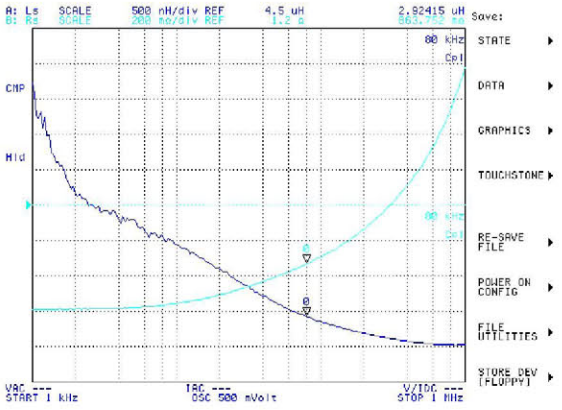

Figure 4. Measured short-circuit resistance and inductance of the transformer prototype.

V. CONCLUSIONS

A method to select the connections of the layers of the windings of planar transformers has been explained. It is adequate to improve the behavior of the component in three aspects, at least: windings power losses reduction, balancing of the current sharing of parallel windings, and voltage drop diminution.

The proposed methodology seems to be a useful tool to select designs based on a chosen criterion. Other aspects of the design, such as the selection of the connections to approach the minimum or the effect of the interleaving on the component capacitances need a further study.

Finally, the methodology has been used to improve the design of the transformer of an actual dc/dc converter. The selected design was built and tested, and the obtained parasitics were adequate for the power topology.

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